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(54) **Semiconductor memory device.**

(57) A semiconductor memory device comprises a memory cell array, a row decoder (RD), a column decoder (CP1), registers (CR) and a control unit (BLW). The control unit (BLW) allows the write operational mode of the column decoder (CD1) to switch. In the ordinary write operational mode, data in the n registers (CR) are written into the active memory cells of the n memory cell columns in one column block (CB) selected by the column decoder, respectively. In the block write mode, data in the n registers are written into active memory cells of the n memory cell columns in the 2^N column blocks selected by the column decoder, respectively.

Another semiconductor memory device comprises N memory units (UNT). Each memory unit (UNT) comprises a memory cell array, a row decoder (RD), a first column decoder (CP1), a second column decoder (CD2), a data input terminal (W/O), registers (CR) and a control circuit. The control circuit is operative to allow the operational mode. When the device is in the ordinary mode, data latched in the register (CR) is written into one memory cell (MC) connected to one word line (WL) selected by the row decoder (RD) of one column selected by the first column decoder (CD1) of column blocks (CB) selected by the second decoder (CD2). While when the device is in the block write mode, data latched in the register (CR) is written at the same time into j memory cells (MC) connected to one word line (WL) selected by the row decoder (RD) of column blocks (CB) selected by the second column decoder (CD2).

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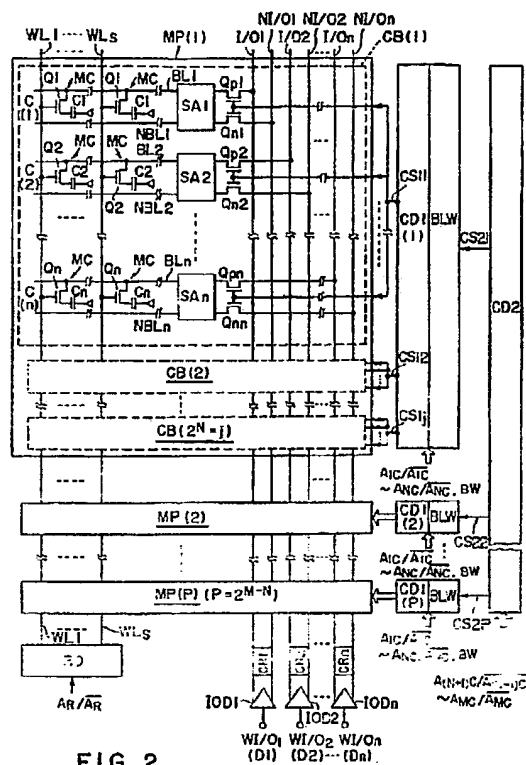


FIG. 2

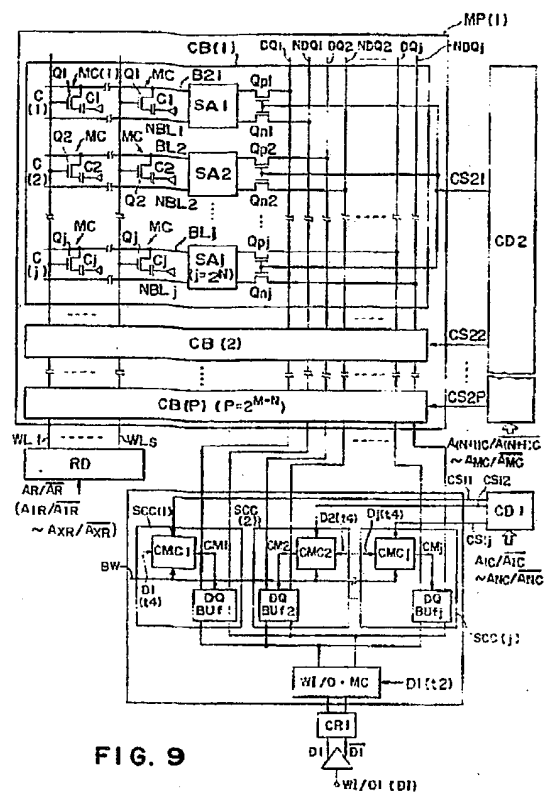


FIG. 9

SEMICONDUCTOR MEMORY DEVICE

FIELD OF THE INVENTION

This invention relates to a semiconductor memory device, and more particularly to a semiconductor memory device suitable when used as a memory for image data for which data rewriting at a high speed is required.

BACKGROUND OF THE INVENTION

FIG. 1 is a block diagram showing the outline of the configuration of a conventional semiconductor memory device. As seen from FIG. 1, in this semiconductor memory device, an address A_R ($= A_{1R} A_{1R} \sim A_{XR} \overline{A_{XR}}$) is inputted to a row decoder RD. The row decoder RD selects one of word lines WL_1 to WL_S ($S=2^x$). Further, a single column decoder CD2 to which addresses $A_{(N-1)C}$ to A_{MC} are inputted selects one of $P (= 2^{M-N})$ column decoders CD1, CD1, Addresses $A_{1C} \overline{A_{1C}}$ to $A_{NC} \overline{A_{NC}}$ are inputted to respective column decoders CD1. Each column decoder CD1 selects one of 2^N column blocks CB in the main section MP. Each column block CB includes n columns C . n data can be inputted to the column block CB and outputted therefrom at the same time. Each column block has so called a column specification of x n bits and 2^N columns. In each column block CB, the memory cell MC is composed of s N-channel MOS transistors Q_1, Q_2, \dots , and s N-channel MOS capacitors C_1, C_2, \dots connected to the respective transistors. These transistors are connected to one of respective bit line pairs BL and NBL and respective word lines WL . n -pairs of bit lines $BL_1, NBL_1; BL_2, NBL_2; \dots$ are connected to n sense amplifiers SA_1, SA_2, \dots , respectively. n sense amplifiers SA_1, SA_2, \dots are connected to n pairs of input lines $I_{01}, NI_{01}; I_{02}, NI_{02}; \dots$ through n pairs of N-channel MOS transistors $Q_{p1}, Q_{p2}, \dots, Q_{n1}, Q_{n2}, \dots$, respectively. n -pairs of input lines $I_{01}, NI_{01}; I_{02}, NI_{02}; \dots$ are connected to n input drivers ID_1, ID_2, \dots , and n data D_1, D_2, \dots are inputted from the respective drivers. On the other hand, column decoders CD1 for control are connected in parallel with the gates of n pairs of transistors, i.e., e.g., the gates of transistors Q_{p1} and Q_{n1} , the gates of transistors Q_{p2} and Q_{n2} , the gates of transistors Q_{p3} and Q_{n3} , the gates of transistors Q_{p4} and Q_{n4} , and the like, respectively. Namely, n columns in one column block CB are simultaneously selected by an output from the decoder CD1.

$WI/01, WI/02, \dots$ denote input/output pins, respectively.

In the above-mentioned device, writing of data into the memory cell is carried out as follows. Namely, n data D_1, D_2, \dots are delivered to n input drivers ID_1, ID_2, \dots , respectively. Further, column addresses $A_{1C} \overline{A_{1C}}$ to $A_{NC} \overline{A_{NC}}$ are delivered to the respective column decoders CD1. In addition, column addresses $A_{(N+1)C} \overline{A_{(N+1)C}}$ to $A_{MC} \overline{A_{MC}}$ are delivered to the column decoder CD2. Thus, it is possible to write, one by one, n data D_1, D_2, \dots into respective n columns by the single access. Namely, n write data D_1, D_2, \dots are delivered to n pairs of input lines $I_{01}, NI_{01}; I_{02}, NI_{02}; \dots$ through n input buffers (input drivers) ID_1, ID_2, \dots . These data are delivered to one of n pairs of bit lines $BL_1, NBL_1; BL_2, NBL_2; \dots$ through n sense amplifiers SA_1, SA_2, \dots from one of n pairs of transistors $Q_{p1}, Q_{n1}; Q_{p2}, Q_{n2}; \dots$ each functioning as a transfer gate. As a result, n data D_1, D_2, \dots are simultaneously written, one by one, into n capacitors (cells) C_1, C_2, \dots through n transistors Q_1, Q_2, \dots by the single access.

In the case of using the semiconductor memory device as constructed above as an image memory, there are many instances where a high speed write cycle using an ordinary write cycle, or a page mode, etc. is used in reading data into the memory. In this case, the number of data which can be written by the single access is n which is the same as the number of input drivers ID_1, ID_2, \dots .

Since the conventional semiconductor memory device is constructed as above, it has drawbacks as described below. Namely, only an extremely small quantity of data can be written by the single access. For this reason, the conventional semiconductor memory device is not suitable for use as an image memory. Namely, since the quantity of write data is small, and the processing speed is low in the case of the above-mentioned conventional memory device even if an attempt is made to satisfy various processing, e.g., painting-out function or color display function, etc., it is difficult to cope with such a requirement.

SUMMARY OF THE INVENTION

With the above in view, this invention has been made, and its object is to provide a semiconductor memory device which can write a large quantity of data therein by the single access.

A semiconductor memory device of this invention comprises a memory cell array including a plurality of memory cells arranged in a matrix manner. Each memory cell is connected to one word line and one bit line. Each word line allows a memory cell connected thereto to be active. One bit line carries out input/output of data with respect to one of the active memory cells. The memory cells are divided into 2^N - (N: a positive integer more than 1) column blocks (CB) every n (n: a positive integer more than 1) columns. The semiconductor memory device further comprises a row decoder responsive to a row address inputted thereto to select one of the word lines, a column decoder responsive to column addresses to select one of column blocks to connect bit lines of memory cells of n columns in the selected column blocks to n data input lines/data readout lines, respectively. The semiconductor memory device further comprises registers which can memorize one bit data applied to input terminals of respective data input lines, provided in the middle of the respective data input lines, and a control unit for allowing a write operational mode of the column decoder to switch between an ordinary write mode and a block write mode in dependency upon level "1" or "0" of a control signal. In the ordinary write operational mode, each column decoder decodes a column address to select only one column block to connect n bit lines in the selected column block to n data input lines, respectively. In the block write mode, each column decoder selects all the 2^N column blocks to connect n bit lines in the column blocks to n data input lines, respectively. Thus, in the above-mentioned ordinary write operational mode, data in the n registers are written into active memory cells in the n memory cell columns in one column block selected by the column decoder. In the above-mentioned block write mode, data in the n registers are written into active memory cells in the n memory cell columns of in the respective 2^N column blocks selected by the column decoder.

Further, a semiconductor memory device of this invention comprises n memory units adapted so that one bit data is applied thereto, the one bit being written into one or a plurality of memory cells, each of the memory units comprising: a memory cell array including a plurality of memory cells arranged in a matrix form, the memory cells being connected to one word lines and one bit lines, respectively, the respective word lines being adapted to allow memory cells connected thereto to be active, one bit line being adapted to carry out input/output of data with respect to one of active memory cells, the memory cells being divided into P ($P=2^{M-N}$) column blocks, the respective column blocks each including j ($j=2^N$) columns; a row decoder responsive to a row address inputted thereto to select one of the word lines; a first column decoder responsive to column addresses applied thereto to decode the addresses to output one of first column select signals; a second column decoder responsive to column addresses inputted thereto to decode the addresses to output one of second column select signals, thus to select one of the column blocks, the second column decoder being operative to connect bit lines of all columns in the selected one column block to one data lines, respectively; a data input terminal adapted so that one bit write data is applied thereto; registers for latching write data applied to the data input terminal; and a control circuit for connecting the registers to the respective data lines, the control circuit being operative to respond to a mode switching signal applied thereto to allow the operational mode to switch between an ordinary mode and a block write mode, wherein when the device is in the ordinary mode, the control circuit responds to one of first column select signals from the first column decoder to connect one of the data lines to the registers, while when the device is in the block write mode, the control circuit is operative to connect all data lines to the registers irrespective of the second column select signals, whereby when the device is in the ordinary mode, data latched in the register is written into one memory cell connected to one word line selected by the row decoder of one column selected by the first column decoder of column blocks selected by the second decoder, while when the device is in the block write mode, data latched in the register is written at the same time into j memory cells (MC) connected to one word line selected by the row decoder of column blocks selected by the second column decoder.

BRIEF DESCRIPTION OF THE DRAWINGS

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In the accompanying drawings:

FIG. 1 is a block diagram showing the outline of the configuration of a conventional semiconductor memory device;

55 FIG. 2 is a block diagram showing the outline of the configuration of a semiconductor memory device according to a general embodiment of this invention;

FIG. 3 is a block diagram showing the outline of the configuration of a semiconductor memory device according to an actual embodiment of this invention;

FIG. 4 is a timing chart for explaining the operation of the configuration of FIG. 3;
 FIGS. 5 and 6 are circuit diagram showing an embodiment of respective blocks of FIG. 2, respectively;
 FIG. 7 is a circuit diagram showing an example of a circuit for generating a signal BW;
 FIG. 8 is a block diagram showing the outline of the configuration according to another embodiment of
 this invention;
 FIG. 9 is a circuit diagram of an embodiment of a portion of the circuit shown in FIG. 8;
 FIG. 10 is a circuit diagram showing an embodiment of respective blocks of FIG. 9; and
 FIG. 11 is a circuit diagram showing an example of the row decoder.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of this invention will now be described with reference to the attached drawings.

FIG. 2 is a block diagram showing the outline of the configuration of a semiconductor memory device according to an embodiment of this invention. In FIG. 2, reference numerals identical to those of FIG. 1 are attached to components equivalent to those of FIG. 1, respectively. The embodiment of FIG. 2 differs from the embodiment of FIG. 1 in that a control unit BLW is provided between decoders CD1 and CD2, and that color registers CR1 to CRn of 1 bit for storing "1" or "0" data are provided in association with the input line pairs. More particularly, input lines I/01 to I/0n and NI/01 to NI/0n are connected to input drivers I0D1 to I0Dn through color registers CR1 to CRn. Data D1, D2, ... are inputted from the drivers I0D1 to I0Dn to the input lines I/01 to I/0n and NI/01 to NI/0n. Between column decoders CD1 and CD2, there is provided a control unit BLW for carrying out a control to switch between the first mode (ordinary mode) for carrying out decoding of $1/2^N$ ($2^N = j$) by addresses $A_{1C}/\overline{A_{1C}}$ to $A_{NC}/\overline{A_{NC}}$ to select one of column blocks CB and the second mode (block write mode) for permitting selection of the 2^N entire column blocks CB at the same time with the addresses $A_{1C}/\overline{A_{1C}}$ to $A_{NC}/\overline{A_{NC}}$ being neglected. This switching is carried out by a block write switching signal BW of 1 bit, for example.

In the device constructed above, the decoder DC2 selects one of decoders DC1. When the ordinary mode is selected by a signal BW, this device operates in a manner similar to that of FIG. 1. In contrast, when the block write mode is selected, a selected decoder CD1 selects all the column blocks CB(1) to CB-(j) connected thereto. Data D1 to Dn in the color registers CR1 to CRn are written, one by one, into one memory cell MC selected by one word line in each of n columns in the respective 2^N column blocks. Namely, writing into $n \times j$ memory cells is carried out.

Detailed examples of the circuit CD2, BLW, CD1 and CR1 to CRn of FIG. 2 are shown in FIGS. 5 and 6.

As seen from FIG. 5, the column decoder CD2 includes P NAND circuits NAND 21 to NAND 2P. Addresses $A_{(N-1)C}/\overline{A_{(N-1)C}}$ to A_{NC} are applied to the respective NANDs. One of NANDs 21 to 2P outputs one of decode signals CS21 to CS2P through one of inverters IV21 to IV2P. The decoders CD1 and the control units BLW have all the same configuration. Namely, e.g., CD1(1), BLW include j NAND circuit NAND 11 to NAND 1j as seen from FIG. 5. Addresses $A_{1C}/\overline{A_{1C}}$ to $A_{NC}/\overline{A_{NC}}$ and a decode signal CS21 are applied to the respective NANDs. An output from the NAND 11 is applied to one input terminal of the control unit BLW through the inverter IV11. A power supply voltage V_{CC} is applied to the other input terminal of the control unit BLW. The control unit BLW functions as a switch. Namely, when the control signal BW is at "0" level, the control unit BLW switches to the a terminal side to provide an output from the inverter IV11 as the decode signal CS11. In contrast, when the control signal BW is at "1" level, the control unit BLW switches to the b terminal side to output the power supply voltage V_{CC} as the signal CS11. Other NANDs, inverters, and the control units are constructed in the same manner as stated above.

Further, other decoders CD1(2) to (P), and the control unit BLW are constructed in the same manner as the above-described decoder CD1(1) and the control unit BLW.

Color registers CR1 to CRn have all the same configuration. For example, color register CR1 is shown in FIG. 6. Namely, this register includes transfer gates T_{CR} connected in series with complementary data lines, respectively, and a pair of inverters IV_{CR} inversely connected in parallel between complementary data lines. If a procedure is taken to apply data D1 to the terminal WI/01 under the state where a pair of transfer gates T_{CR} are caused to be turned ON thereafter to allow the pair of gates T_{CR} to be turned off, data applied earlier is registered into the color register CR1.

FIG. 3 shows an example of so called $\times 8$ bits and 4 columns wherein, in the device of FIG. 2, N is set to 2, i.e., the number of column blocks CB is set to four, and n is set to 8, i.e., data simultaneously inputted/outputted have D1 to D8 of 8 bits.

The operation of the device of FIG. 3 will now be described.

The decoder CD2 selects one of decoders CD1.

In the ordinary mode, column addresses A_{1C} and A_{2C} are decoded by a selected decoder CD1. Thus, one of four column blocks CB is selected.

On the other hand, in the block write mode, a block write switching signal BW is delivered to the control unit BLW. Thus, decoding of column addresses $A_{1C}/\overline{A_{1C}}$, $A_{2C}/\overline{A_{2C}}$ by the column decoder CD1 is neglected.

5 Four column blocks CB are selected at the same time. In this case, as data subjected to block write, data stored and set in advance into the color registers CR1 to CR8 are used in place of data D1 to D8 inputted to the input drivers IOD1 to IOD8 in the block write cycle.

The timings of this block write is shown in FIG. 4. Namely, at timing t2, a row address (C) and a mask data (G) are established. In this instance, when the column address strobe CAS (B) is at H level, DT/OE (E) is at H level, and DSF (F) is at L level, the operational mode enters the block write mode.

10 Alternatively, at timing t4, column addresses $A_{3C}/\overline{A_{3C}}$ to $A_{8C}/\overline{A_{8C}}$ (C) and a column select (G) are established. In this instance, when DSF (F) is at H level, the block write operation is executed. In this connection, the column address input at the time of fall (t4) of the column address strobe \overline{CAS} (B) is $A_{3C}/\overline{A_{3C}}$ to $A_{8C}/\overline{A_{8C}}$ inputted to the column decoder CD2. The addresses A_{1C} and A_{2C} inputted to the column decoder CD1 become ineffective address data.

When this device is in a block write mode, it is permitted to have a mask function. As shown in the timing chart of FIG. 4, ON/OFF operation of the mask function in the I/O direction is carried out by a level of $\overline{WB}/\overline{WE}$ (D) at the time of fall of the row address strobe \overline{RAS} (A) at timing t2. Namely, when $\overline{WB}/\overline{WE}$ (D) is at L level, the mask function in the I/O direction becomes effective or valid. By levels of input data D1 to D8 at this time, masking in the I/O direction is carried out. Namely, when data D1 to D8 are at H level, masking in the I/O direction is not effective. When data D1 to D8 are at L level, masking in the I/O direction is enabled. Further, masking in the column direction is carried out by data D1 to D4 (G) when the column address strobe \overline{CAS} (A) falls at time t4.

Tables 1 and 2 show examples of mask functions in the I/O and column directions at the time of block write. As shown in Table 1, where input data D1 to D8 are "01100111", masking is applied to data corresponding to input data D1, D4 and D5 as shown in Table 2. On the other hand, where column block select data selected by input data D1 to D4 are "1101", masking is applied to the column 3 as shown in Table 2. As a result, where "00110101" is written in advance into color registers CR1 to CR8 through input drivers IOD1 to IOD8, the contents of the color registers CR1 to CR8 are written into bits and columns which are not subjected to masking as shown in Table 2.

Table 2 shows the following fact in relation to FIG. 2. Namely, it is now assumed that the decoder DC2 selects the decoder DC(1), and that the control unit BLW selects the block write mode. At the time when the mask function is inoperative, data "00110101" (see Table 1) stored in advance into the color registers CR1 to CR8 are written into four column blocks CB(1) to CB(4), respectively. Namely, when attention is drawn to, e.g., column block CB(1), data of "0", "0", "1", "1", "0", "1", "0", "1" are written, one by one, into memory cells MC belonging to the columns C(1) to C(8) of memory cells MC selected by a word line WL1, respectively. This is the same in connection with respective columns C(1) to C(8) of column blocks CB(2) to CB(4). On the contrary, where the mask function is caused to be operative, so the result is as shown in Table 2, data write operation will be conducted as follows. Namely, writing into any columns C(1) to C(8) in the column block CB(3) is not carried out. Namely, data remain in respective original states. In the column blocks CB(1), CB(2) and CB(4), writing into the columns C(1), C(4) and C(5) is not carried out. Thus, when attention is drawn to, e.g., the column block CB(1), data of "0", "1", "1", "0", "1" in the color registers CR2, CR3, CR6, CR7 and CR8 are written into memory cells belonging to columns C(2), C(3), C(6), C(7) and C(8). In contrast, writing into memory cells belonging to other columns C(1), C(4) and C(5) is not carried out.

Input data D1 to D8 can be arbitrarily set.

TABLE 1

INPUT DATA	MASK DATA	COLUMN BLOCK SELECT DATA	CONTENTS OF COLOR REGISTERS CR1 TO CR8
D1	0	1	0
D2	1	1	0
D3	1	0	1
D4	0	1	1
D5	0		0
D6	1		1
D7	1		0
D8	1		1

TABLE 2

COLUMN	COLUMN BLOCK CB(1)	COLUMN BLOCK CB(2)	COLUMN BLOCK CB(3)	COLUMN BLOCK CB(4)
C(1)	MASK	MASK	MASK	MASK
C(2)	0	0	MASK	0
C(3)	1	1	MASK	1
C(4)	MASK	MASK	MASK	MASK
C(5)	MASK	MASK	MASK	MASK
C(6)	1	1	MASK	1
C(7)	0	0	MASK	0
C(8)	1	1	MASK	1

The above-mentioned control signal BW is generated by a circuit shown in FIG. 7. for example In the figure, signals BRIN, BCIN and DSIN applied to NANDs are signals synchronous with the rising and falling of the signals \overline{RAS} , \overline{CAS} and \overline{DSF} , respectively.

FIG. 8 is a block diagram showing the entire configuration of a different embodiment according to this invention.

The circuits of respective bits have all the same configuration. The first bit (W1/01) section (first memory unit UNIT(1)) will be chiefly described. Addresses $A_{(N+1)C}$, $\overline{A}_{(N+1)C}$ to A_{MC} , \overline{A}_{MC} are inputted to the second column decoder CD2. As a result, one of decode signals CS21 to CS2P is outputted as a decode signal. The decode signal thus obtained is applied to the memory unit MP(1). A column control circuit CC(1) is connected to the memory unit MP(1). One of decode signals CS11 to CS1j from the first column decoder CD1 is applied to the circuit CC(1). Namely, the decoder CD1 responds to addresses A_{1C} , \overline{A}_{1C} to A_{NC} , \overline{A}_{NC} applied thereto to decode them to output one of decode signals CS11 to CS1j. An input/output pin W1/01 is connected to the control circuit CC(1) through the color register CR1 and the driver IOD1. Other memory units UNIT(2) to (UNIT(n)) are similar to the above.

A portion of the circuit of FIG. 8 is shown in FIG. 9 in a more practical manner. Namely, FIG. 9 shows

the detail of the portion of the first unit UNIT(1). Further, the control circuit CC includes j subcontrol circuits SCC corresponding to the number j of columns in the respective column blocks CB, and one W/O mask control W/O*MC. Each subcontrol circuit SCC includes a switching circuit CMC and a DQ buffer DQ Buf.

The details of the first column decoder CD1, the control circuit CC and the color register CR1 are shown in FIG. 10.

The decoder CD1 includes j NAND circuits NAND 11 to 1j. Addresses A_{1C} to A_{jC} or $\overline{A_{1C}}$ to $\overline{A_{jC}}$ are applied to respective NANDs. Each output is connected to the control circuit CC through one of inverters IV11 to IV1j.

A decode signal CS11 from the decoder CD1(1) and input data D1 to the input/output pin W/O1 are inputted in parallel to the switching circuit CMC1 in respective subcontrol circuits SCC in the control circuit CC. This switching circuit CMC1 switches between the signals CS11 and D1 to output it as an output CM1 in dependency upon the level "1" or "0" of the control signal. This output CM1 is applied to the DQ buffer DQ Buf 1. In dependency upon the level "1" or "0" of CM1, the buffer DQ Buf 1 is placed in the states where the input is connected to the output and is cut off therefrom, respectively.

The color register CR1 has the same configuration as that of the color register shown in FIG. 6. Namely, this register includes transfer gates T_{CR} respectively connected in series with complementary data lines, and a pair of inverters IV_{CR} inversely connected in parallel between complementary data lines.

Further, the row decoder RD is constructed as shown in FIG. 11, for example.

The device of FIGS. 8 to 10 operates in a manner similar to the devices which has been described with reference to FIGS. 2 to 7. Namely, this device has the same operational mode (the ordinary operational mode and the block write mode), and are permitted to have column direction mask and/or I/O direction mask in the block write mode, respectively.

The ordinary operational mode will be first described.

When the device is in this mode, one memory cells MC are selected every respective W/O by the decoders RD, CD1 and CD2. Data stored in advance in the color registers CR1 to CRn are written into the selected one memory cells MC, respectively.

Namely, when attention is drawn to the first bit, as seen from FIG. 9, the row decoder RD selects one of word lines WL1 to WLS. It is now assumed that the word line WL1 is selected. Further, the column decoder CD2 outputs one of decode signals CS21 to CS2P. It is assumed that this decoder outputs, e.g., a decode signal CS21 to allow j columns C(1) to C(j) in the memory block CB(1) to be active. The column decoder CD1 outputs one of decode signals CS11 to CS1j. It is assumed that, e.g., a decode signal CS11 is outputted. That signal CS11 is applied to the switching circuit CMC1. As seen from FIG. 10, a control signal BW is also applied to this circuit CMC1. When the device is in the ordinary operational mode, this signal BW is at "0" level. For this reason, the level "1" of the input signal CS11 is applied to the buffer DQ Buf 1 as an output CM1. Thus, the buffer DQ Buf 1 is switched to ON state (a terminal side). On the other hand, the W/O mask control W/O*MC is switched to ON state (non-masking state) by the "1" level signal of data D1 (t_2) applied to the pin W/O1 at time t_2 of FIG. 4. Thus, data D1 stored in advance into the color register CR1 is written into the memory cell MC(1).

The block write mode will now be described.

In the case of this mode, when attention is drawn to the first bit, data stored in advance into, e.g., the color register CR1 is written at the same time into j memory cells in the column block CB(1) of memory cells connected to the word line shown in FIG. 9. Data of the second to the n -th bits are written in a manner similar to the above.

Namely, it is now assumed that row decoder RD selects a word line WL1, that the first column decoder CD2 outputs a signal CS21, and that the second column decoder CD1 outputs a signal CS11. In this mode, the control signal BW is set to "1". For this reason, the switching circuits CMC1 to CMCj are all switched to the D1 side (b terminal side). D1 at time t_4 (FIG. 4) is taken in as the D1. In this mode, at time t_4 , D1 is at "1" level. For this reason, "1" is applied to the buffers DQ Buf 1 to DQ Buf j as the CM1. For this reason, all the buffers DQ Buf 1 to DQ Buf j are brought into ON state. On the other hand, at time t_2 , D1 is applied to the W/O mask control W/O*MC. For this reason, the mask control W/O*MC is in ON state. For this reason, data D1 stored in advance into the color register CR1 is written into j memory cells connected to the word line WL1 of memory cells in the column block CB(1).

In the above-mentioned block write mode, masking in the I/O direction and masking in the column direction can be applied.

Masking in the I/O direction in the block write mode will be first described.

As seen from FIG. 9, data D1 is applied, as a control signal, to the W/O mask control W/O*MC corresponding to the input pin W/O1. Namely, data $Dn(t_2)$ applied at time t_2 is applied, as a control signal, to the pin W/On of the mask control W/O*MC corresponding to the n -th bit. When the device is simply in

the block write mode, all of n data $D1(t_2)$ to $Dn(t_2)$ are at "1" level at time t_2 . However, in the case of applying masking in the I/O direction, it is sufficient to allow an arbitrary one of n data $D1(t_2)$ to $Dn(t_2)$ to be "0". In the memory unit MP corresponding to the mask control $WLO \cdot MC$ to which data $Dn(t_2)$ of "0" is applied, data write operation is not carried out.

5 The masking in the column direction in the block write mode will be conducted as follows.

Namely, this masking will be described with reference to FIG. 9, for example. It is sufficient to apply data of "0" level, as data $Dj(t_4)$ at time t_4 , to an arbitrary one of switching circuits $CMC1$ to $CMCj$. Thus, e.g., "0" data is applied to the buffer DQ Buf 1. As a result, the buffer DQ Buf 1 is switched to OFF state (FIG. 10). Thus, data in the color register $CR1$ is not propagated to the data line $DQ1$ and $NDQ1$. Thus, 10 even if writing into the memory cells in the columns $C(2)$ to $C(j)$ within, e.g., the column block $CB(1)$ is carried out, writing into the memory cells belonging to the column $C(1)$ is not carried out. Namely, masking in the column direction is applied.

Explanation has been made by drawing attention to only a portion of the circuit for facilitating understanding. However, it is to be noted that write operations in respective modes are carried out in other 15 portions having similar configuration in a manner similar to the above.

The explanation which has been given with reference to FIG. 4 and tables 1 and 2 in connection with the first embodiment (FIGS. 2 and 3) applies to that in connection with the second embodiment (FIG. 8) as it is.

As described above, in accordance with this embodiment, data having a quantity 2^N times larger than 20 that of RAM by the single access can be written. If the data quantity is the same, write speed 2^N times higher than that of RAM can be realized. For example, with respect to the block write in the case of a four column specification, N is equal to 2. Thus, data quantity $2^2 (= 4)$ times larger than in the prior art can be written at a time. Further, the block write is very effective for particularly the processing of painting out of a square area of the image processing. For example, where the I/O direction is caused to be in correspond- 25 ence with the pixel direction, in the block write of 8 bit configuration and four column specification, data can be simultaneously written into 8×4 pixels. Further, by using the mask function, the processing on the boundary between areas can be very simply implemented at a high speed. In addition, in the case of using I/O as color information, 8 of 8×4 bits and 4 thereof may be used as color information and data in the pixel direction, respectively.

30 From the foregoing description, in accordance with this invention, same data can be written into respective columns of a plurality of column blocks. Accordingly, the data quantity which can be written by the single access is increased, thus making it possible to write data at a high speed. In addition, a delicate control of write data can be made by the mask function. Accordingly, a semiconductor memory device effective for image storage or image processing is provided.

35 Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A semiconductor memory device comprising:

40 a memory cell array including a plurality of memory cells (MC) arranged in a matrix form, said memory cells being connected to one word lines (WL) and one bit lines (BL), respectively, said respective word lines being adapted to allow memory cells connected thereto to be active, one bit line being adapted to carry out input/output of data with respect to one of active memory cells, said memory cells being divided into 2^N (N : a positive integer more than 1) column blocks (CB) every n (n : a positive integer more than 1) columns.

45 a row decoder (RD) responsive to a row address ($A_R, \overline{A_R}$) inputted thereto ($A_R, \overline{A_R}$) to select one of said word lines,

a column decoder (CD) responsive to column addresses ($A_{1C}, \overline{A_{1C}}$ to $A_{MC}, \overline{A_{MC}}$) inputted thereto to select one of column blocks (CB), said column decoder being operative to connect bit lines of memory cells of n columns in the selected column blocks to n data input lines/data input lines/data readout lines, respectively.

50 registers (CR) provided in the middle of said respective data input lines, said registers being adapted so that one bit data applied to input terminals (W/O) of said respective data input lines can be stored therein, and

a control unit (BLW) for allowing a write operational mode of said column decoder (CD1) to switch between an ordinary write mode and a block write mode in dependency upon a level of "1" or "0" of a control signal 55 (BW), wherein when said device is in said ordinary write operational mode, said column decoder (CD1) decodes a column address to select only one column block to connect n bit lines in the selected column block to n data input lines, respectively, while when said device is said block write mode, said column decoder (CD1) selects all 2^N column blocks to connect n bit lines in said column blocks to n data input

- lines, respectively, and wherein when said device is in said ordinary write operational mode, data in said n registers (CR) are written into active memory cells in the n memory cell columns in one column block (CB) selected by said column decoder, while when said device is in said block write mode, data in said n registers are written into active memory cells of the n memory cell columns in the 2^N column blocks selected by said column decoder, respectively.
2. A device as set forth in claim 1, which further comprises a first mask control circuit operative so that when one of "1" and "0" level data is applied to the input terminals (WI/O) of said respective data input lines, writing from said respective registers (CR) into said memory cells is executed, while when the other level data is applied, said writing is not executed.
3. A device as set forth in claim 1, which further comprises a second mask control circuit adapted so that when said device is in said block write operational mode, said device is operative so that selection by said column decoder (CD) of a column block (CB) corresponding to one of "1" and "0" of input data of an arbitrary number of n input terminals of said input terminals (WI/O) of said data input lines is allowed, and that selection by said column decoder (CD1) of a column block (CB) corresponding to the other thereof is inhibited.
4. A device as set forth in claim 1, which further comprises P column decoders (CD1), said 2^N column blocks (CB) being connected to said column decoders, respectively, one of said P column decoders (CD1) being selected by a main column decoder (CD2), main column addresses ($A_{(N-1)C}, \overline{A_{(N-1)C}}$ to $A_{MC}, \overline{A_{MC}}$) being applied to said main column decoder (CD2).
5. A semiconductor memory device comprising N memory units (UNIT) adapted so that one bit data is applied thereto, said one bit data being written into one or a plurality of memory cells (MC), each of said memory units (UNIT) comprising:
a memory cell array including a plurality of memory cells (MC) arranged in a matrix form, said memory cells being connected to one word lines (WL) and one bit lines (BL), respectively, said respective word lines being adapted to allow memory cells connected thereto to be active, one bit line being adapted to carry out input/output of data with respect to one of active memory cells, said memory cells being divided into P column blocks (CB), said respective column blocks (CB) each including j columns,
a row decoder (RP) responsive to a row address (A_R) inputted thereto to select one of said word lines,
a first column decoder (CD1) responsive to column addresses ($A_{1C}, \overline{A_{1C}}$ to $A_{NC}, \overline{A_{NC}}$) applied thereto to decode said addresses to output one of first column select signals (CS11 to CS1j),
a second column decoder (CD2) responsive to column addresses ($A_{(N-1)C}, \overline{A_{(N-1)C}}$ to $A_{MC}, \overline{A_{MC}}$) inputted thereto to decode said addresses to output one of second column select signals (CS21 to CS2P), thus to select one of said column blocks (CB), said second column decoder being operative to connect bit lines (BL) of all columns in the selected one column block to one data lines (DQ), respectively,
a data input terminal (WI/O) adapted so that one bit write data is applied thereto, registers (CR) for latching write data applied to said data input terminal (WI/O),
a control circuit for connecting said registers (CR) to said respective data lines (DQ), said control circuit being operative to respond to a mode switching signal (BW) applied thereto to allow the operational mode to switch between an ordinary mode and a block write mode, wherein when said device is in said ordinary mode, said control circuit responds to one of first column select signals (CS11 to CS1j) from said first column decoder (CD1) to connect one of said data lines (DQ) to said registers (CR), while when said device is in said block write mode, said control circuit is operative to connect all data lines (DQ) to said registers (CR) irrespective of said second column select signals (CS11 to CS1j), whereby when said device is in said ordinary mode, data latched in said register (CR) is written into one memory cell (MC) connected to one word line (WL) selected by said row decoder (RD) of one column selected by said first column decoder (CD1) of column blocks (CB) selected by said second decoder (CD2), while when said device is in said block write mode, data latched in said register (CR) is written at the same time into j memory cells (MC) connected to one word line (WL) selected by said row decoder (RD) of column blocks (CB) selected by said second column decoder (CD2).
6. A device as set forth in claim 5, wherein said respective control circuits (CC) include column direction mask circuits (SCC) responsive to j column direction mask control signals ($D1(t4)$ to $Dj(t4)$) applied thereto when said device is in said block write mode to selectively cut off connections between said registers (CR) and j data lines (DQ).
7. A device as set forth in claim 5 or 6, wherein said respective control circuits (CC) include I/O direction mask circuits ($WI/O \cdot MC$) responsive to one I/O direction mask control signal ($Dn(t2)$) applied thereto when said device is in said block write mode to cut off the connection between said registers (CR) and all of j data lines (DQ).
8. A device as set forth in claim 5, wherein said respective control circuits (CC) include j column direction

- circuits (SCC), said respective mask circuits being connected in series between said respective data lines (DQ) and said registers (CR), each of said respective mask circuits (SCC) comprising: a first switch circuit (CMC) to which one of first column select signals (CS11 to CS1j) from said first decoder (CD1), one of j column direction mask control signals (D1(t4) to Dj(t4)), and said mode switching signals (BW) are applied, said first switch circuit being operative to output either one of column select signals (CS11 to CS1j) or one of column direction mask control signals (D1(t4) to Dj(t4)) in dependency upon the level of said mode switching signal (BW); and a second switch circuit (DQ Buf) to which an output (CM) from said first switch circuit (CMC) is applied, said second switch circuit being operative to carry out ON/OFF operation of connections between said data lines (DQ) and said registers (CR).
9. A device as set forth in claim 5, wherein said registers (CR) include latch circuits comprised of two inverters (IV_{CR}) inversely connected in parallel, and transfer gates (T_{CR}), respectively, said transfer gates being operative to carry out ON/OFF operation of connections between said data input terminals and said latch circuits.
10. A device as set forth in any one of claims 5 to 8, wherein transfer gates (Q_pQ_n) are connected between said respective data lines (DQ/NDQ) and said respective bit lines (BL,NBL), each of said transfer gates (Q_pQ_n) being operative to be conductive when one of second column select signals (CS21 to CS2P) from said second column decoder (CD2) is applied thereto.

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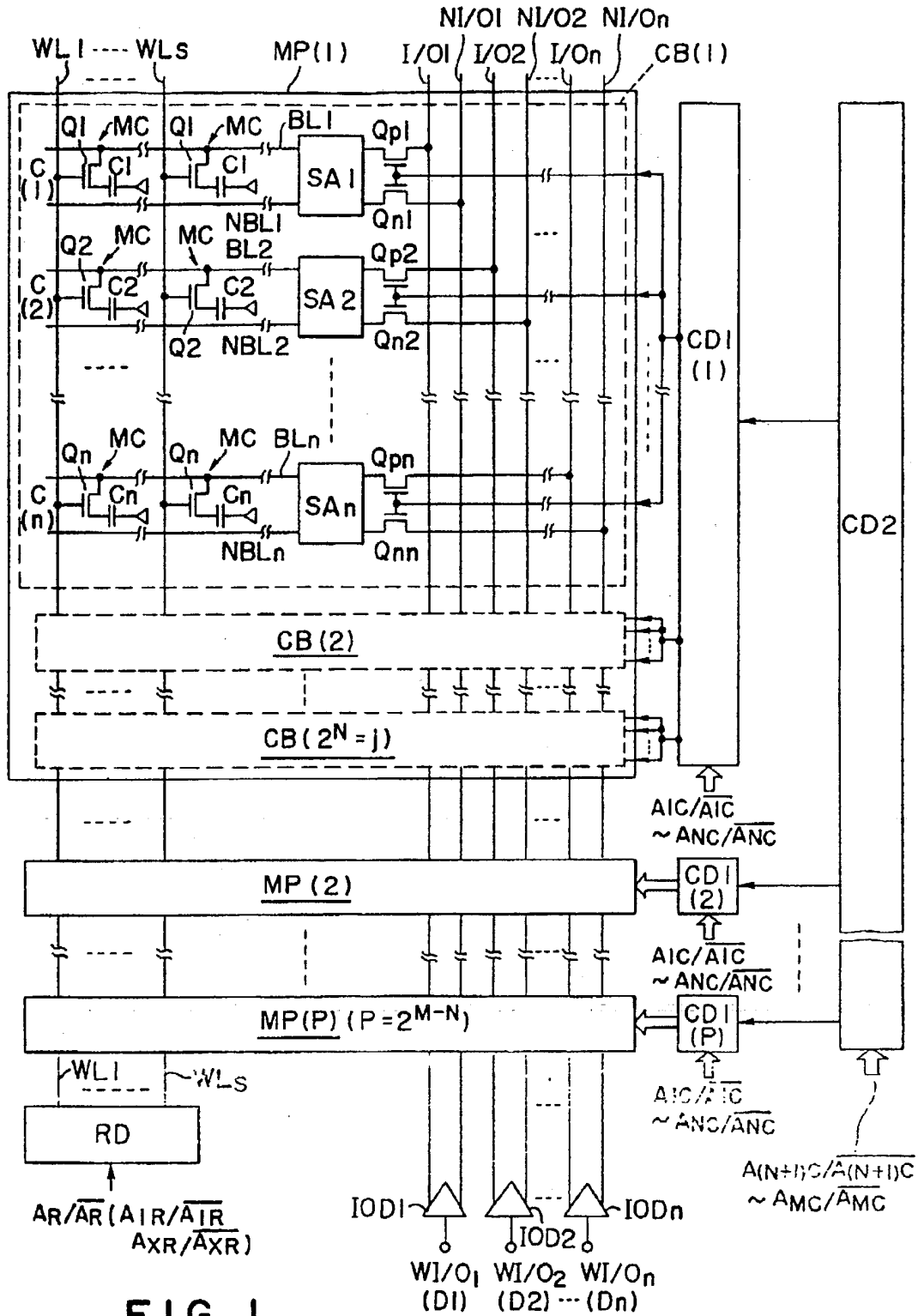
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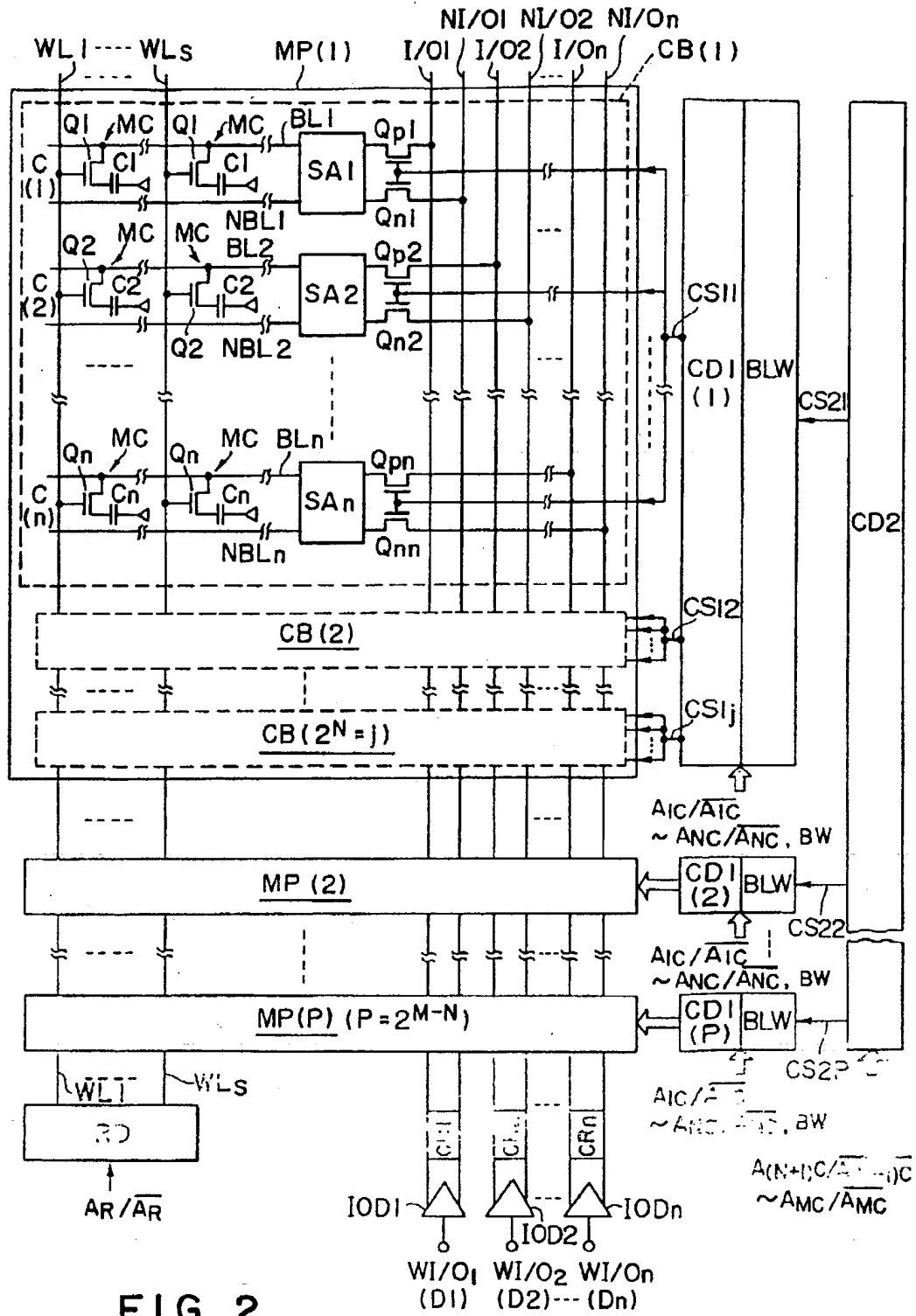
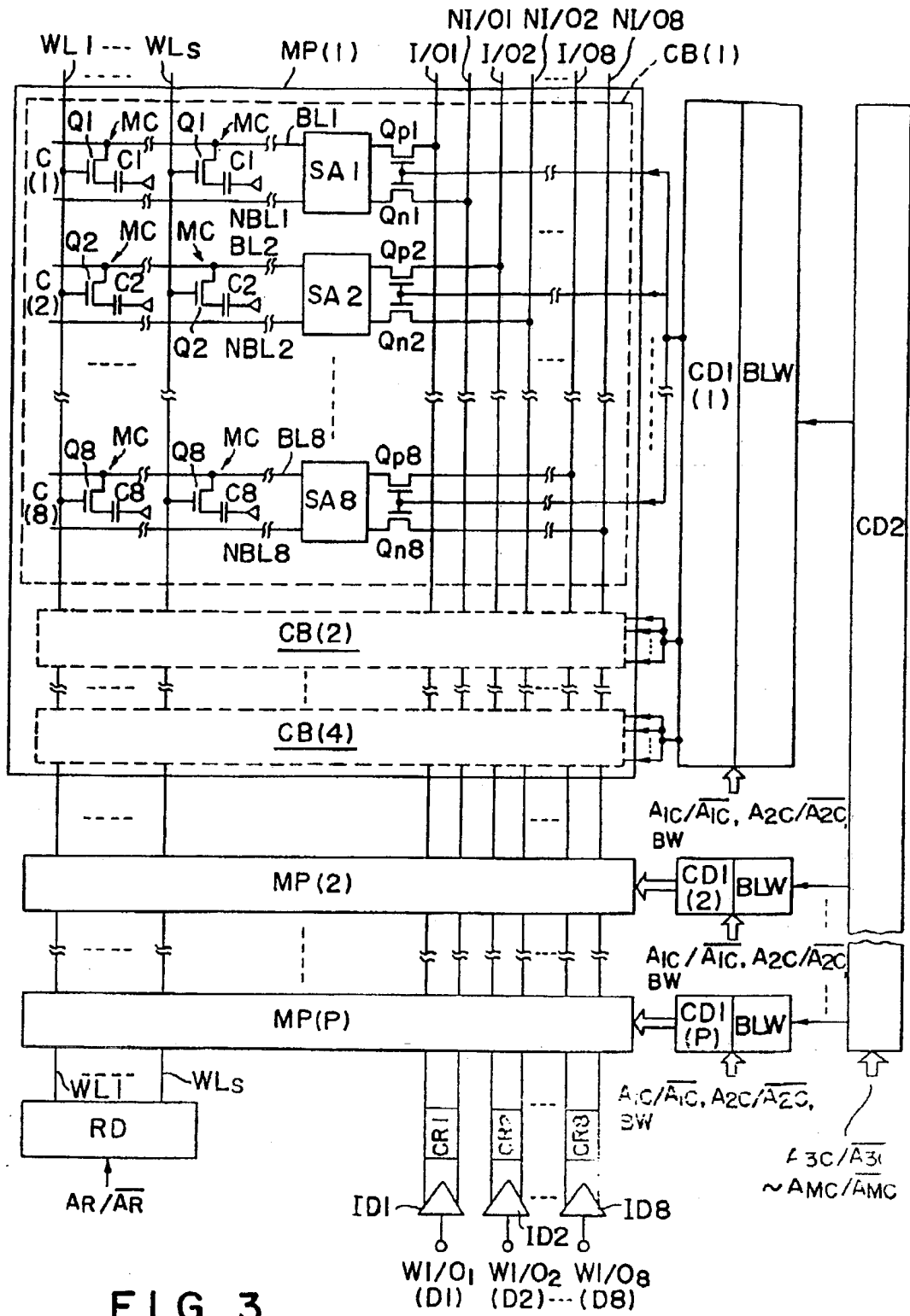


FIG. 2



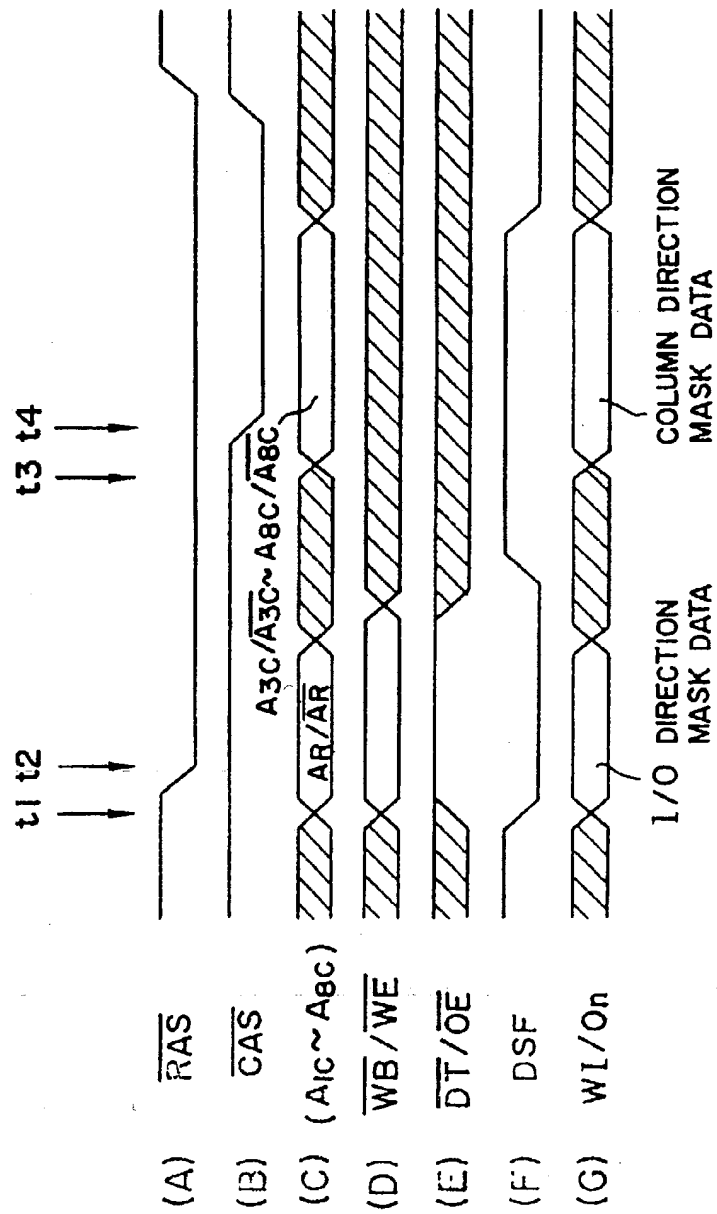


FIG. 4

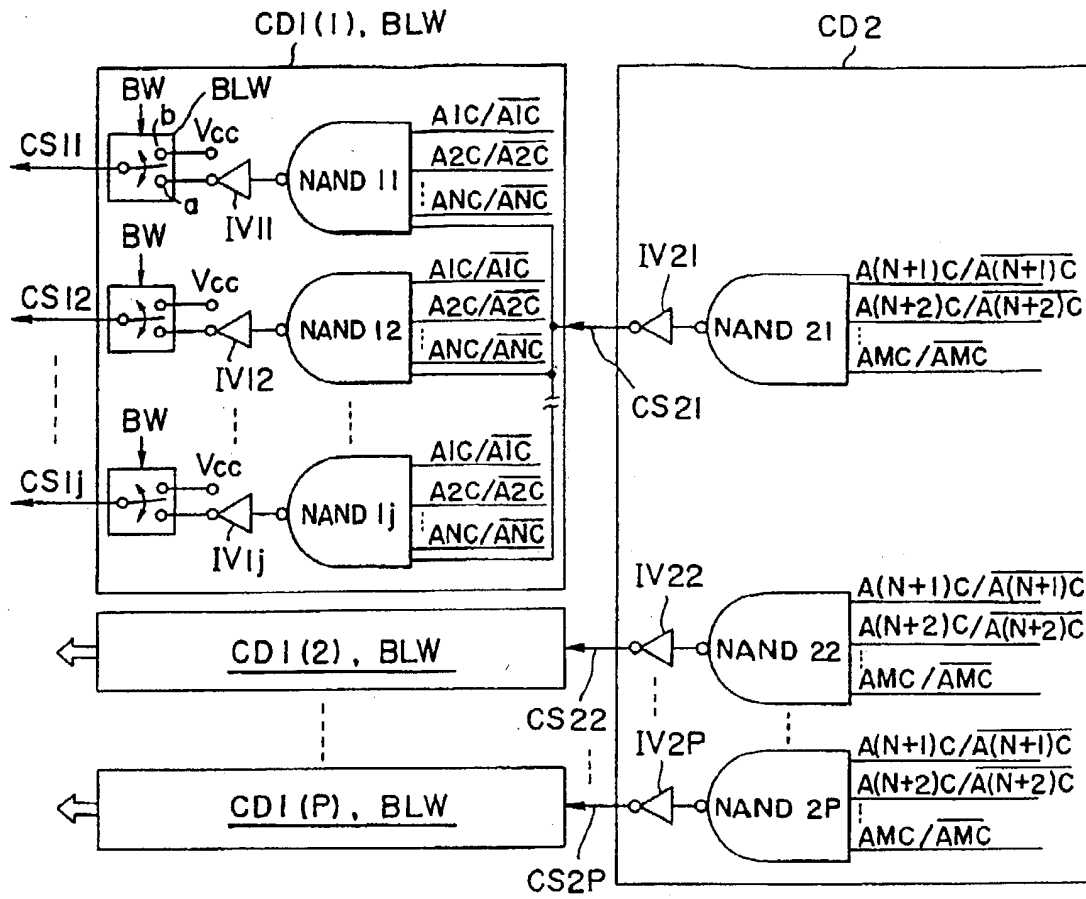


FIG. 5

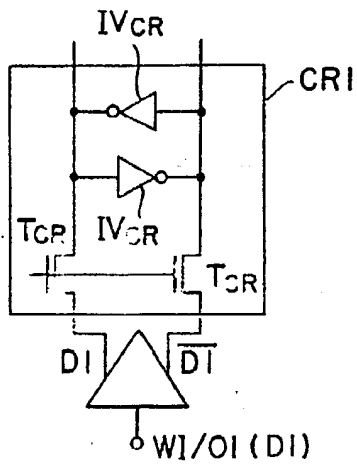


FIG. 6

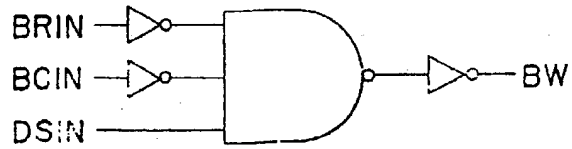


FIG. 7

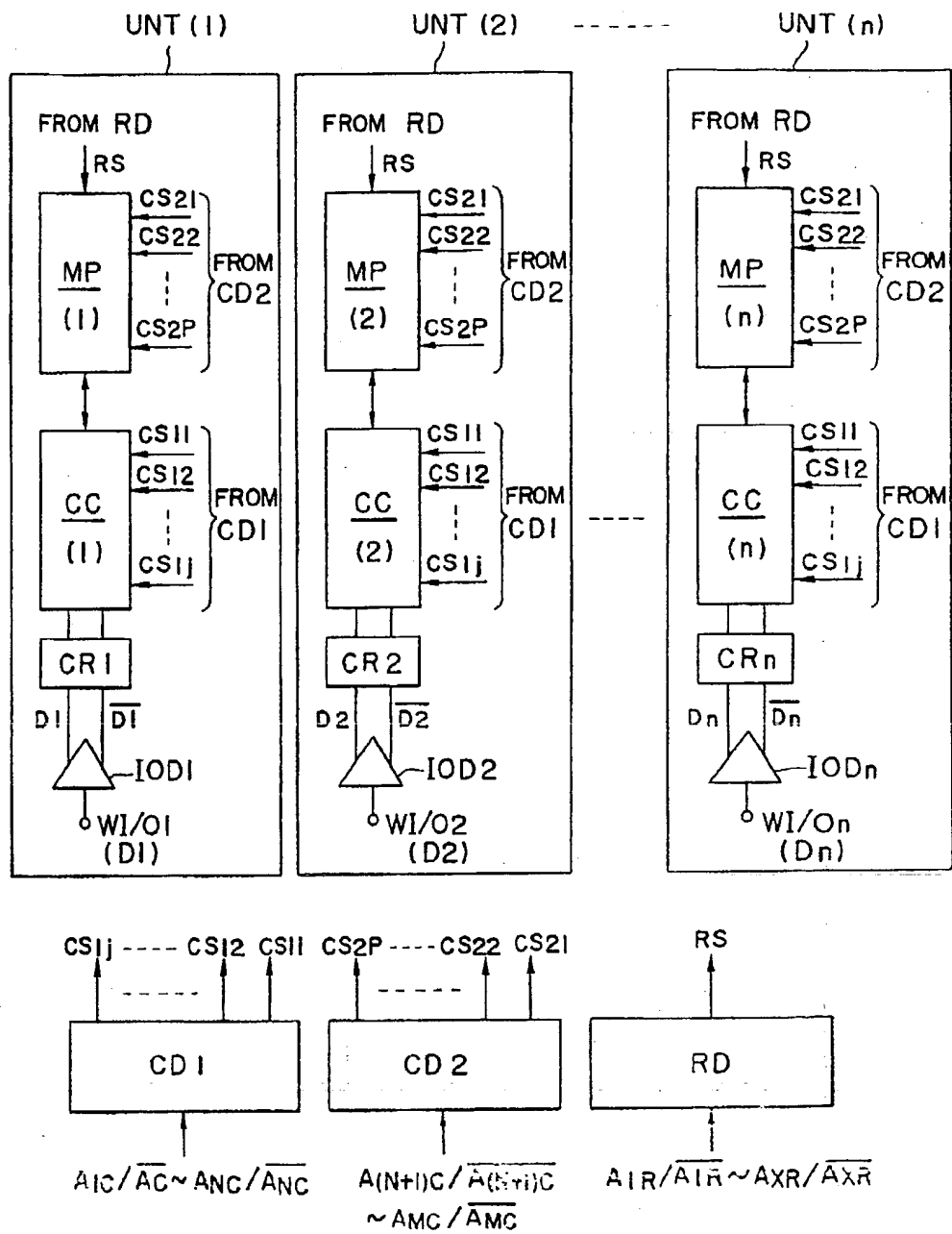


FIG. 8

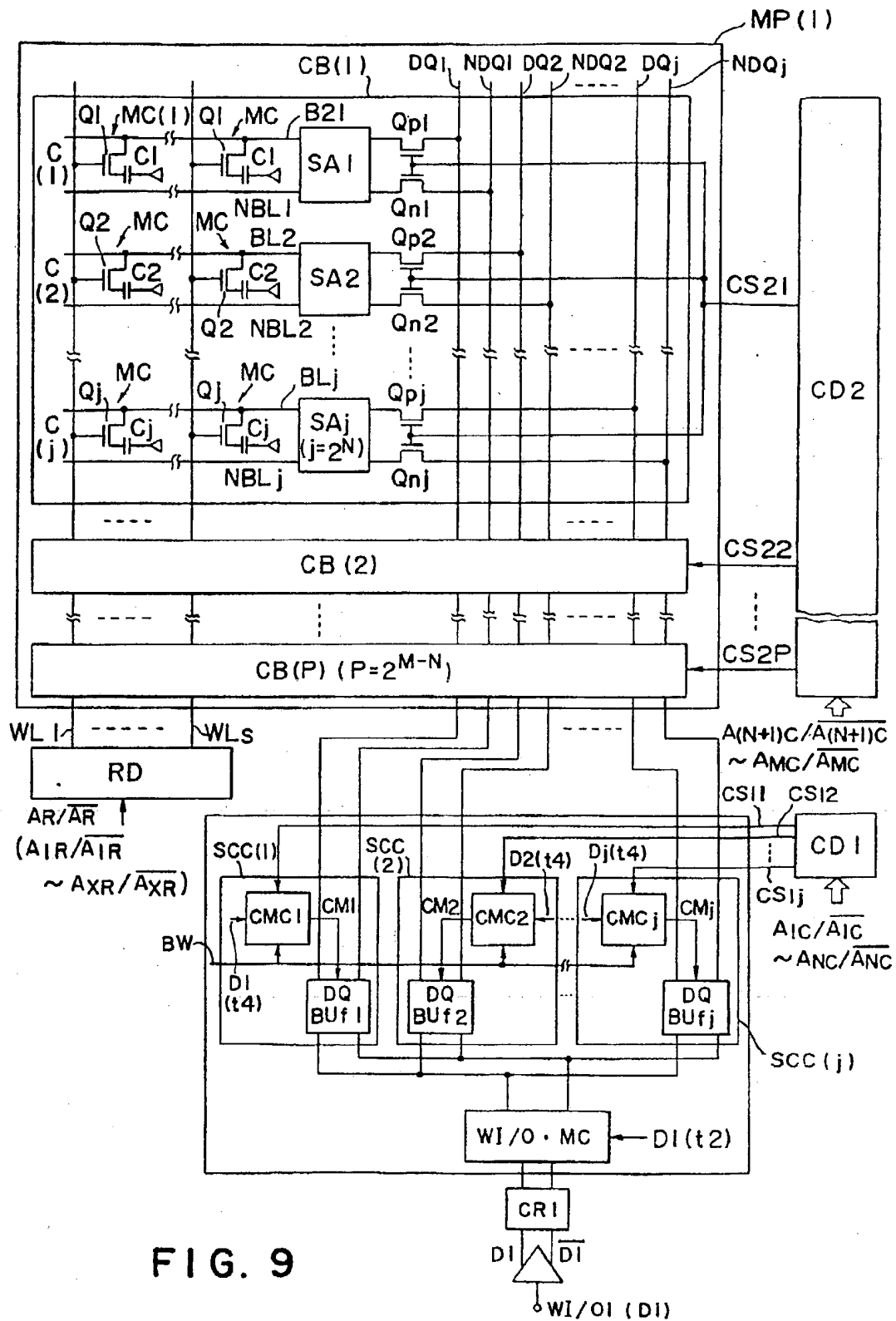


FIG. 9

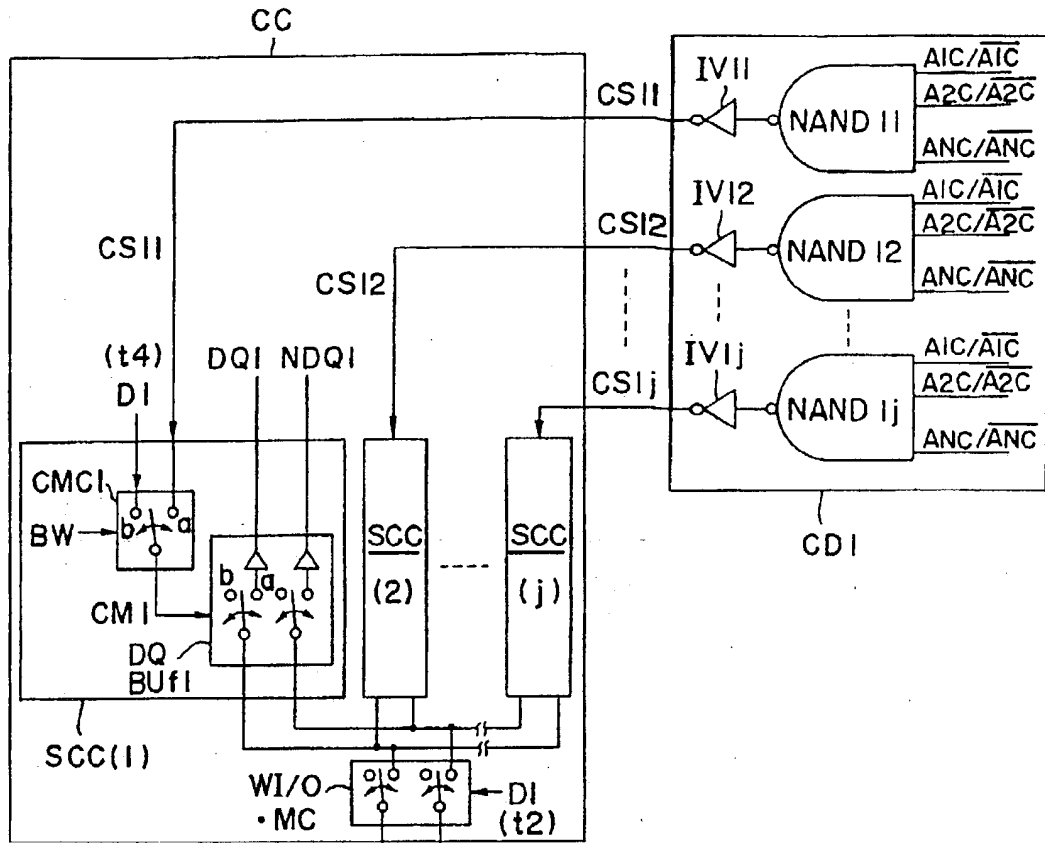


FIG. 10

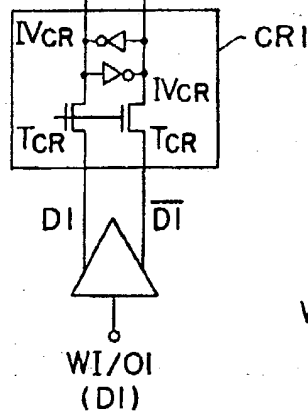


FIG. 11

